

# **EUV Lithography**

## **Transition from Research to Commercialization**

**Charles W. Gwyn and Peter J. Silverman**  
**EUV LLC and Intel Corporation**

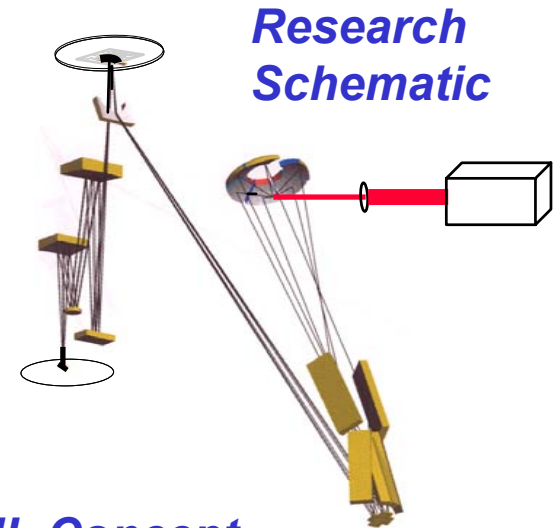
Photomask Japan 2003  
Pacifico Yokohama, Kanagawa, Japan

# EUV Lithography

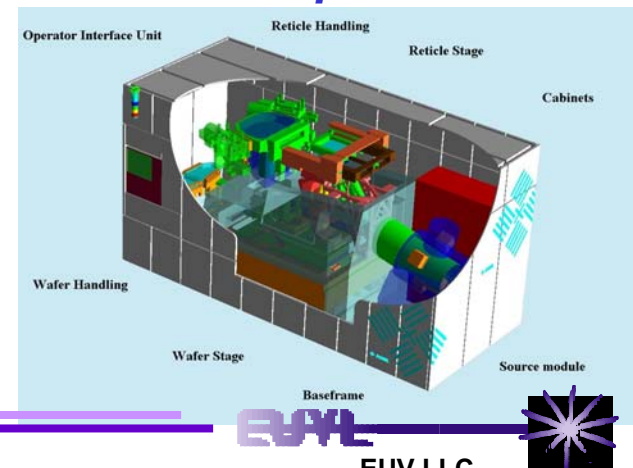
## Transition from Research to Commercialization

### Outline

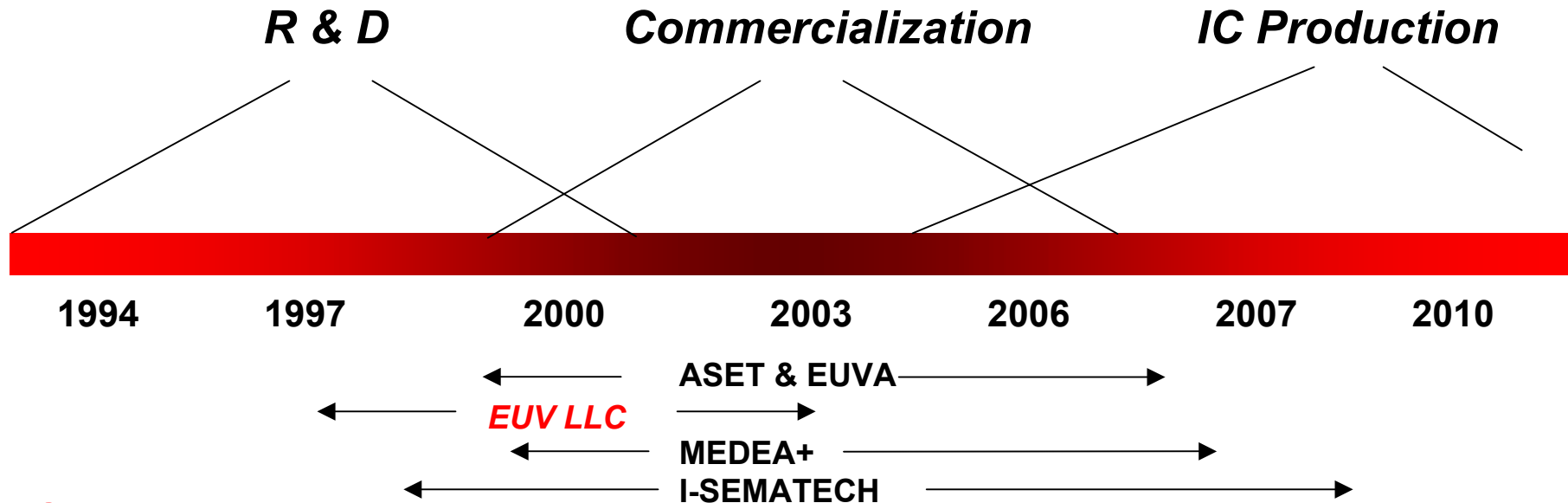
- Background
- Technology Description
- Research results and status
- Commercialization status
  - Source
  - Tools
  - Masks
- World wide focus
- Remaining challenges
- Summary



### *ASML Concept*



# Phases of EUVL implementation



## Objectives

- Perform basic R & D
- Develop and integrate modules into alpha tool
- Demonstrate EUVL printing & quantify needed improvements

- Develop beta and preproduction tools
- Implement improvements with selective R&D
- Establish infrastructure for masks, resists, and Metrology equipment

- Manufacture production tools
- Scale up infrastructure
- Continuous improvement

# EUV LLC Research and Development

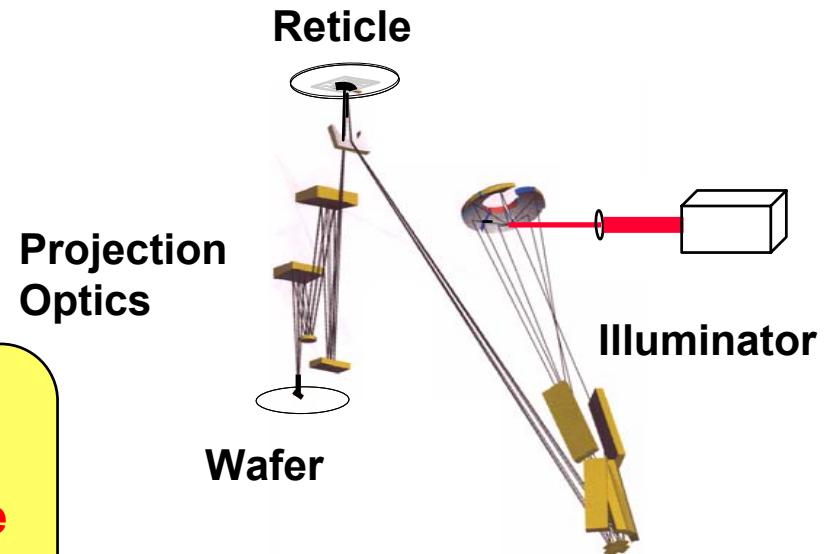
## Strategy

Develop the unique modules required for EUV Lithography:

- Reflective Projection Optics and Condenser
- EUV Source
- Environmental Control Systems
- Mask Blanks and Masks
- Resist

### Goal

**Demonstrate the feasibility of EUV Lithography by building a prototype 100nm EUV Lithography exposure tool**



# EUVL R & D requirements different than conventional lithography

*Reticle Stage*

Aspheric mirrors with sub-nm surface error

EUV reflective masks

Robust 4X reduction EUV reflective projection optics

*Illuminator*

A reliable source of EUV photons

A condenser to collect and shape EUV radiation

*Wafer Stage*

- Multilayer reflective coatings for mirrors
- Environmental control system
- EUV resist
- Operating and control software
- Precision Metrology

# Modules integrated into demonstration alpha tool



**Reticle Stage**

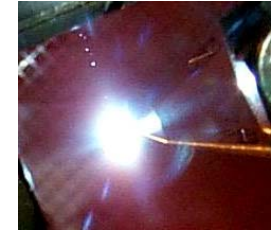
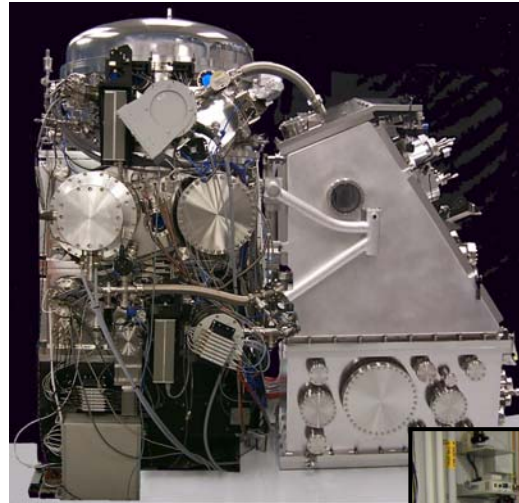


**PO Box**

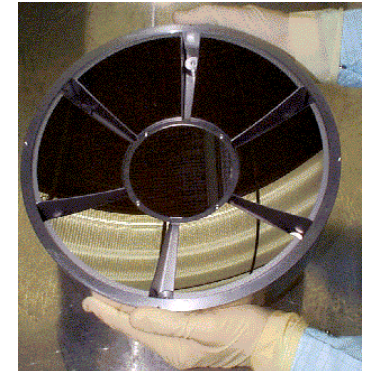


**Wafer Stage**

**Engineering Test Stand**



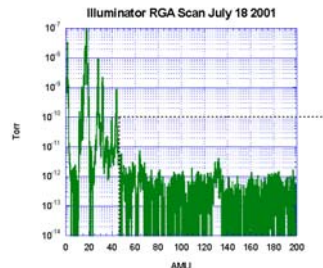
**Laser Plasma Source**



**Condenser Optic**



**Control &  
Data Acquisition**



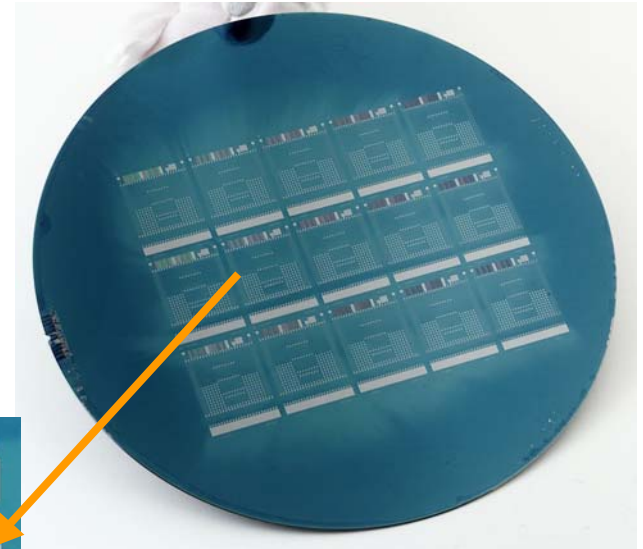
**Environment  
Control**



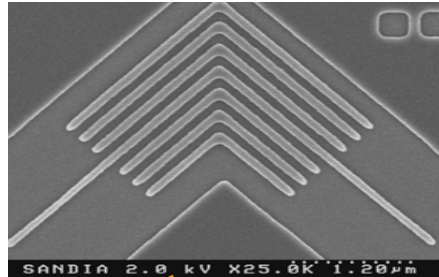


# Full field Images produced by 0.1 NA ETS

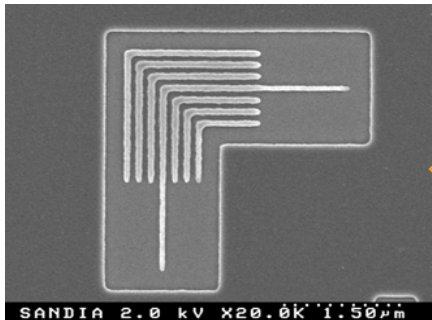
200 mm Wafer



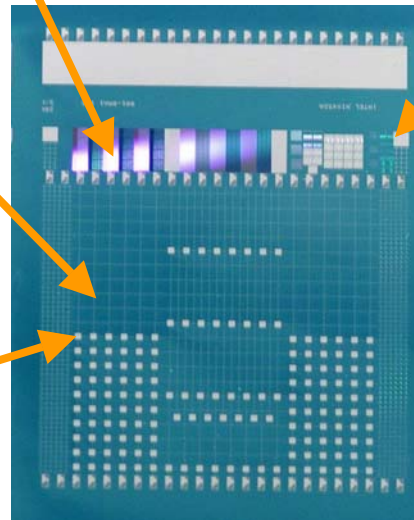
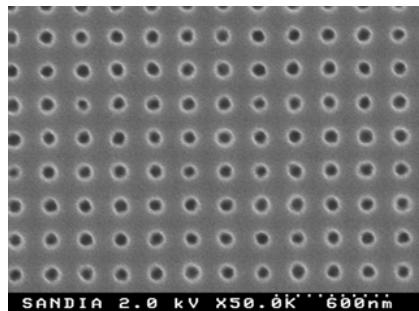
100 nm Elbows 1:1



80 nm Elbows 1:1



100 nm contacts 1:1



24 x 32.5 mm<sup>2</sup> field



# R & D Exposure Systems

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System (type)	Location	NA/ Magnification	Field size Min. Res.	Lens quality	Reticle Size
ETS Scanner	Livermore, CA	0.1 4 x	24 x 32 mm <sup>2</sup>	$\lambda/20$	6 inch sq.
10x Microstepper	Livermore, CA	0.1/10 x	0.5 x 0.5 mm	$\lambda/40$	1.25 x 1.06 in wafer
BESSY MET static	Berlin, Germany	0.3/5x	200x600 microns <sup>2</sup>	$\lambda/10$	8 inch wafer
BEL static	Grenoble, France	0.3/10x	100x200 microns	$\lambda/10$	8 inch wafer 6 x 6 inch reticle
ASET static	Atsugi, Japan	0.3/5x	300 x 500	$\lambda/7$	8 inch wafer
MET (static)	Berkeley, CA	0.3/5x	200 x 600	$\lambda/40$	6 inch reticle

Other capabilities include a 10x interferometric exposure capability at Berkeley and at the U. of Wisconsin

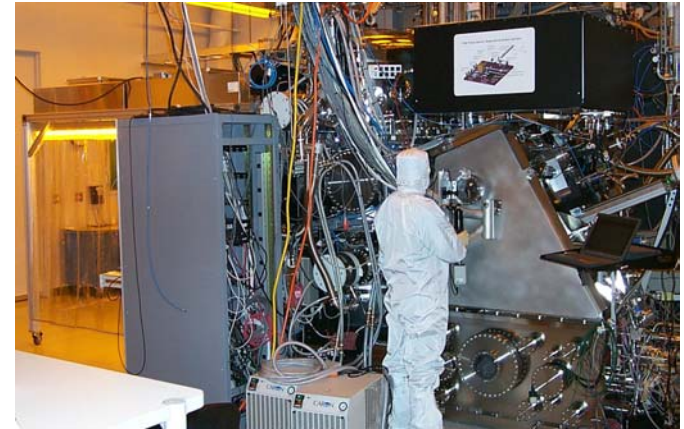


# R & D Status

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## *Technology:*

- All elements of technology demonstrated
  - Full field scanning alpha tool
  - Mask fabrication & repair
  - Experiments correlate with models
  - Metrology for optics and masks
- Key decisions made, e.g. wavelength, mask format, engineered multilayers, etc.
- Tools are available for continued learning



## *R & D activity:*

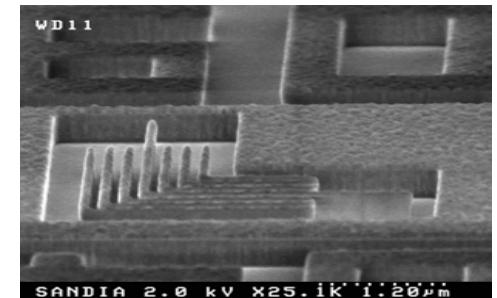
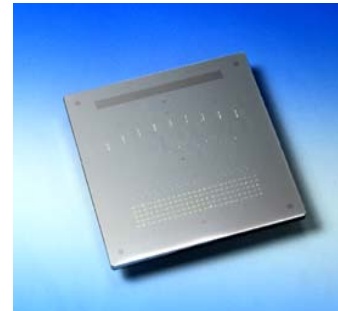
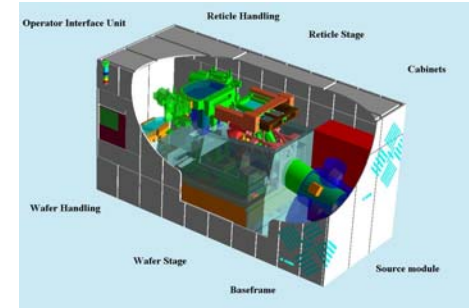
- VNL available for technology transfer
- Individual LLC members continuing selective R & D
- Universities actively pursuing projects
- I-SEMATECH establishing Mask Development Center in Albany, NY

## *Needs:*

- Continued improvement for all areas and reduced CoO

# Commercialization focusing on three areas

- **Tools**
  - **EUV Source**
    - Discharge
    - Laser Plasma
  - **Beta tools**
    - Microstepper
    - Stepper scanners
- **Masks**
  - Blanks
  - Patterned masks
  - Metrology
- **Resists**



# Electric Discharge Source

## *Technology:*

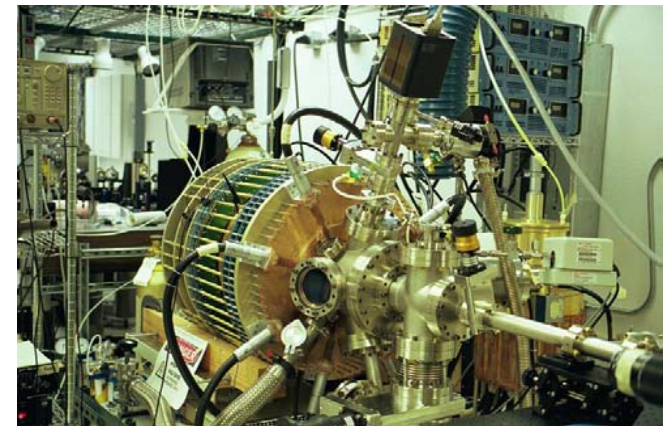
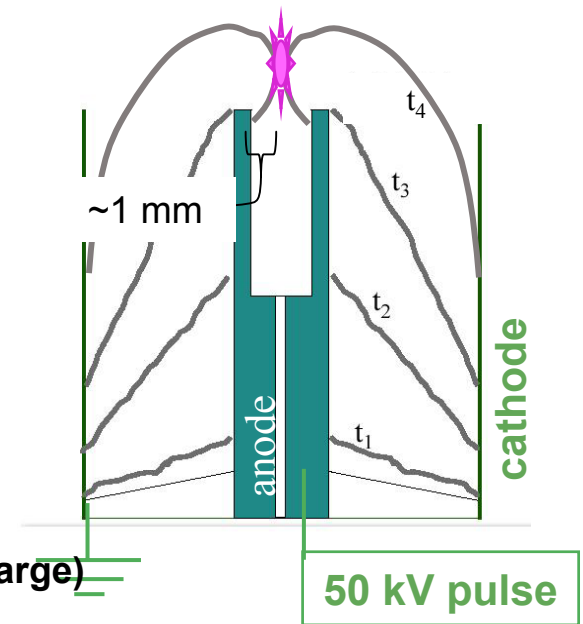
- Pulsed electrical discharge creates plasma in presence of Xe gas
- Plasma-wall proximity increases thermal and erosion problems
- Collected EUV power =  $\frac{\text{Input electrical power}}{(\text{collector efficiency})(\text{wall to discharge})}$
- Up to 17 W at intermediate focus @ 6kHz burst mode
- Issues: Electrode lifetime and debris
- Sn considered as alternate to Xe target

## *Commercial status:*

- Systems operating only in burst mode
- Leading systems: Cymer, Xtreme, Philips

## *Production Needs:*

- Higher power, multiplexed sources
- Improved conversion/collection efficiencies
- Improved CoO

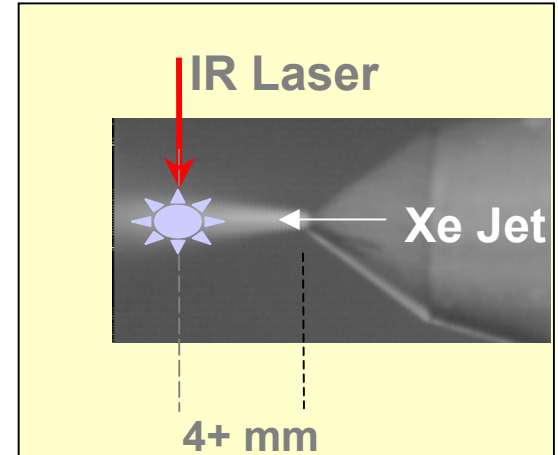


Cymer DPF System

# Laser-Produced Plasma Source

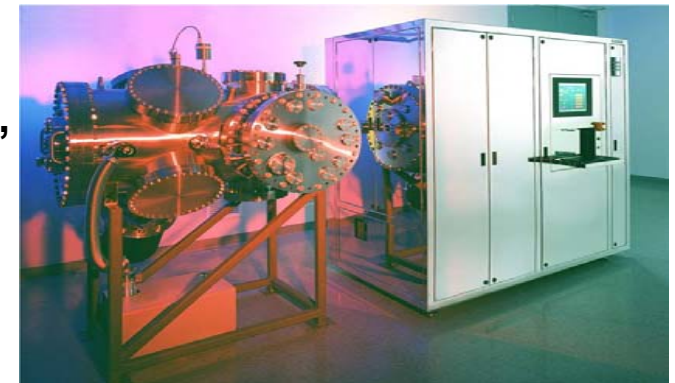
## *Technology:*

- Pulsed IR laser focused on Xe gas, liquid or solid target creates plasma
- Good plasma-wall separation: helps thermal erosion
- Relatively inefficient EUV generation (multiple steps)
- Collected EUV power = 
$$\frac{\text{Input electrical power}}{(\text{collector efficiency})(\text{laser to EUV})(\text{wall to laser})}$$
- Sn being considered as alternate for Xe target



## *Commercial status:*

- Leading system: CEO/TRW  
4.5 KW LPP laser developed, 3 chains tested,  
22 W EUV in  $2\pi$  with filament jet, 9.4 W, 0.87% eff.,  
at intermediate focus with 2.4 KW laser
- Active development for 6 systems by Japanese, European, and US companies
- Sn considered as an alternate target



CEO 4.5 KW System

## *Production Needs:*

- Higher power
- Improved conversion/collection efficiencies

# Exposure EUVL tools

## *Technology:*

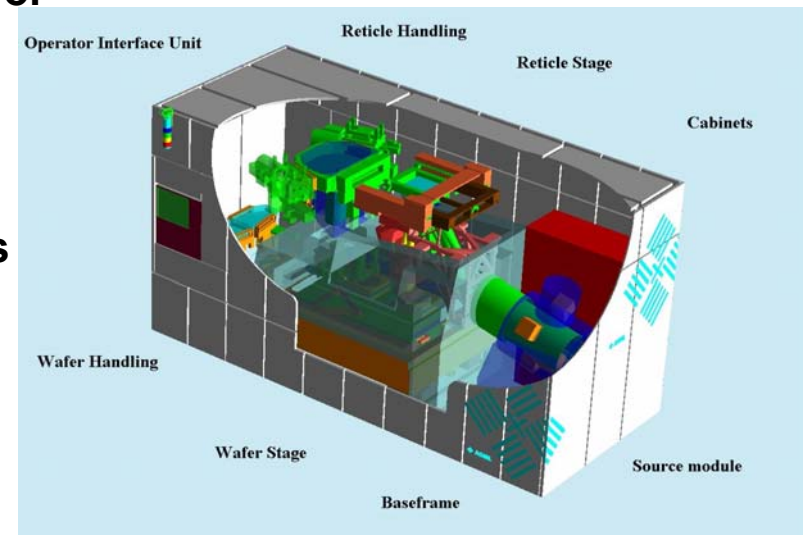
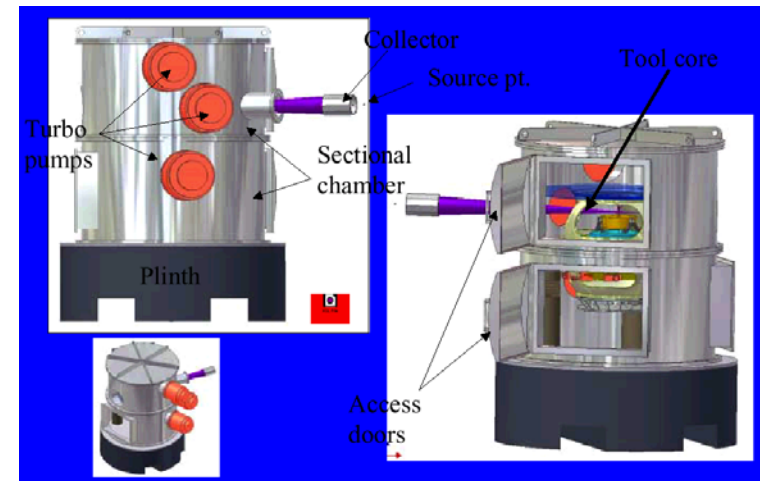
- Complete tools validate technology feasibility - ETS and other R & D tools,
- All modules/processes demonstrated – optics, multilayers, metrology, stages, vacuum operation

## *Commercial status:*

- Exitech developing 0.3 NA microsteppers for process development – deliveries in 04
- ASML, Nikon and Canon developing beta and production tools
- Over 100 companies and laboratories working on subsystems and components

## *Production Needs:*

- Accelerated schedule for tools
- Additional infrastructure suppliers



# Mask Development

## Strategy:

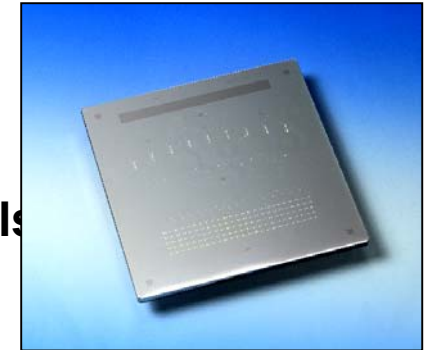
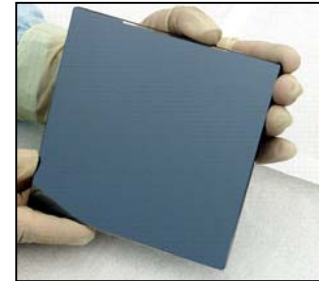
### Mask Blanks

- Use LTEM polished blanks
- Cover and repair defects
- Deposit low defect multilayers
- Inspection and repair defects
- Absorber deposition

### Mask Patterning

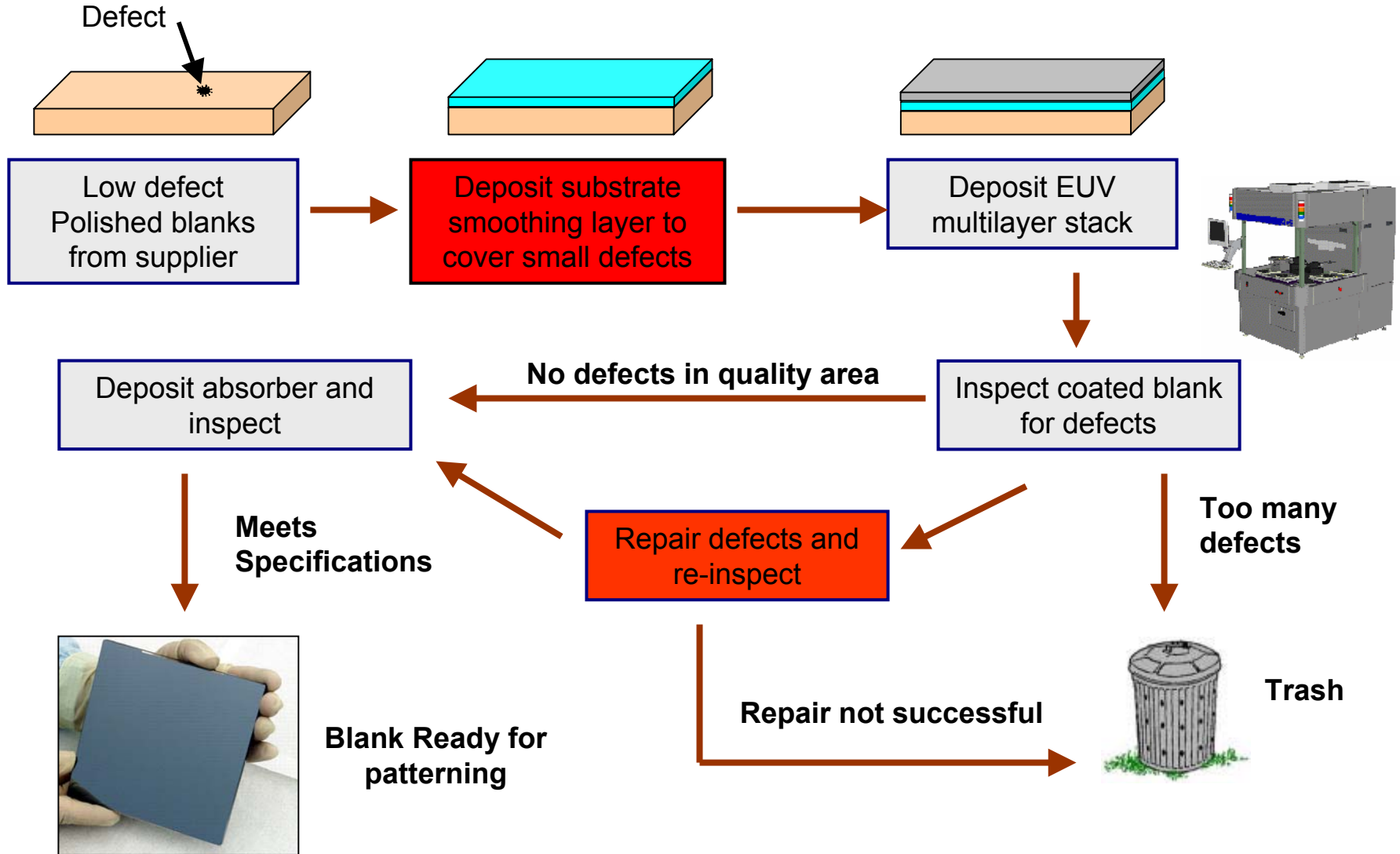
- Use conventional ebeam writing
- Extend/adapt conventional inspection tools
- Use FIB or ebeam for repair
- Use removable protection cover

### Affordable mask costs



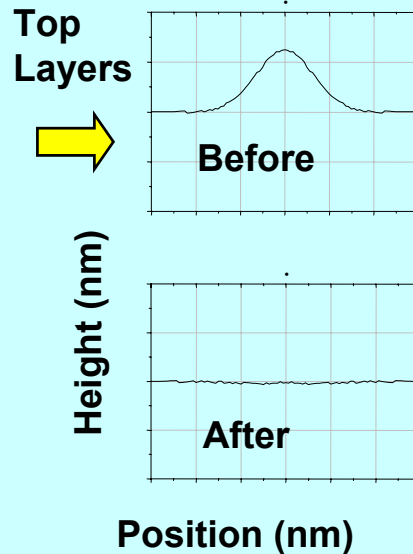


# Mask blank manufacturing process



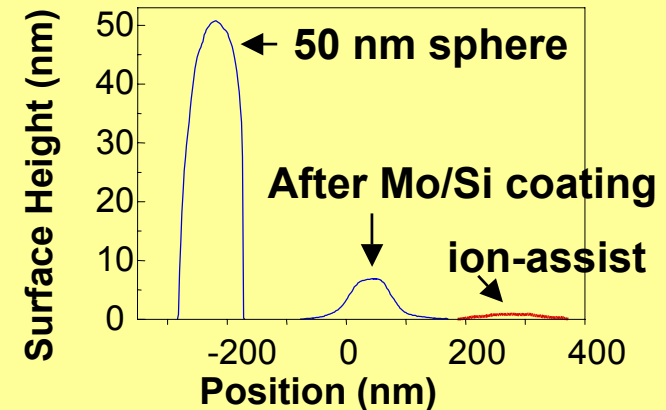
# Mask Blank Defect Repair

## Phase defect repair

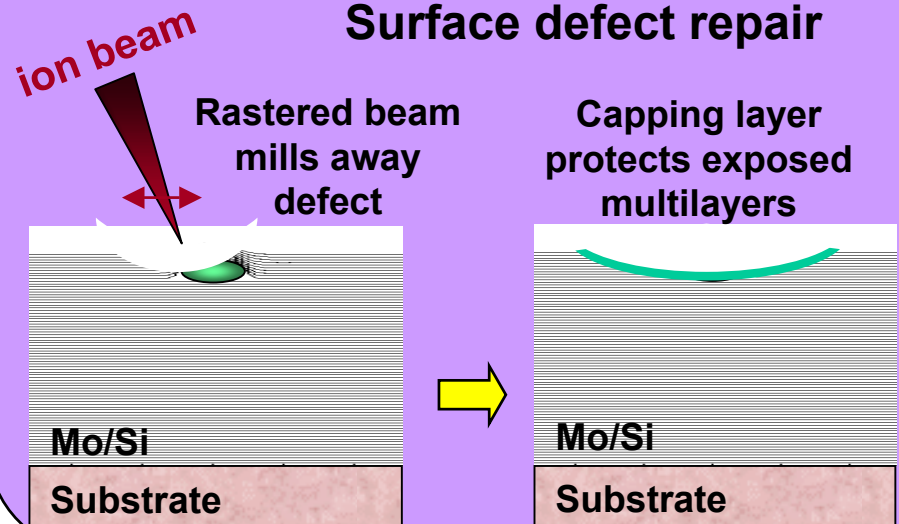


Localized heating and ML contraction controlled by adjusting e-beam dose

## Substrate defect smoothing



## Surface defect repair



# Mask Blank production

## *Technology;*

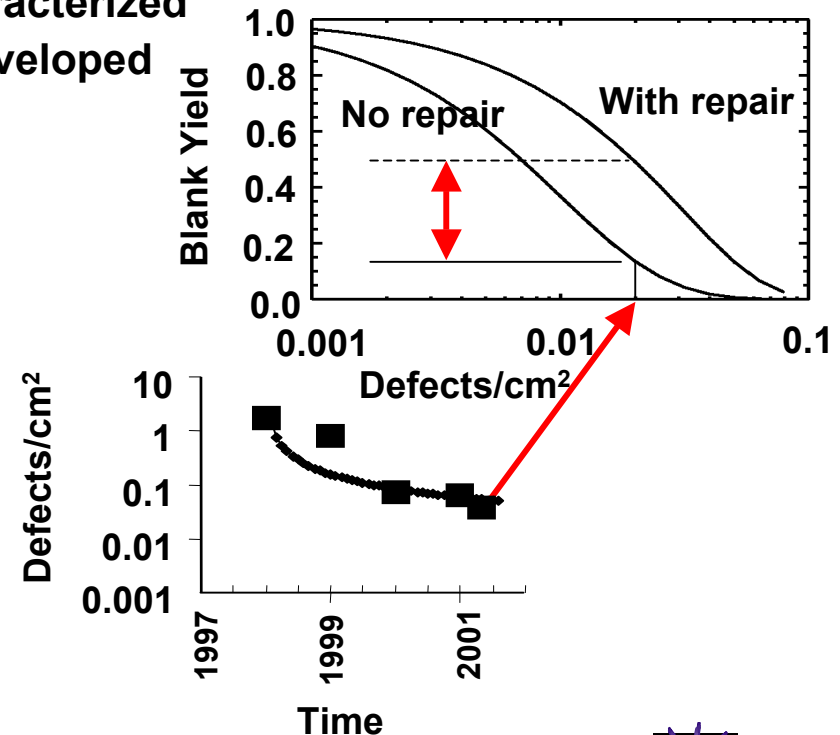
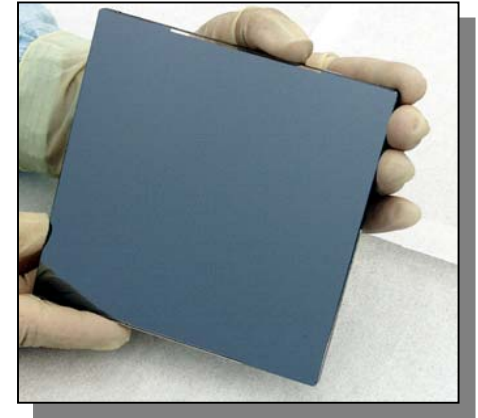
- LTEM or Zerodur materials - SEMI standard P37
- Blanks polished to <200 nm flatness
- Models developed and applied for stress, flatness, and chucking effects
- LTEM mask materials identified and characterized
- Defect mitigation and repair methods developed

## *Commercial status:*

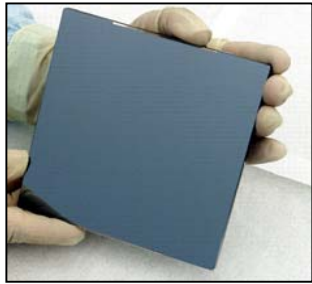
- Schott Lithotech, Asahi, Hoya, Corning developing blanks
- I-SEMATECH establishing mask blank development center in Albany, NY

## *Production needs:*

- Improved blank flatness – 50 nm
- Combined inspection/repair tool
- Reduced costs



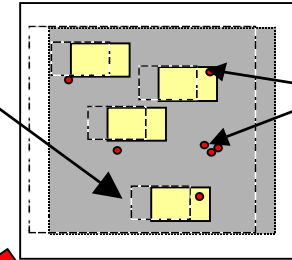
# Mask patterning steps



Mask blanks from supplier

Deposit resist and prebake

Shift Mask Pattern to Cover one or more defects



Mask Blank defects

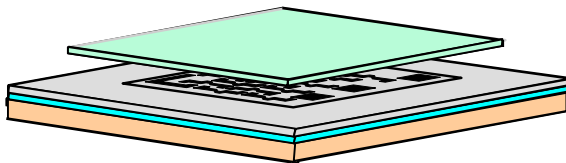
E-beam write, Etch & Clean

Inspect patterned masks

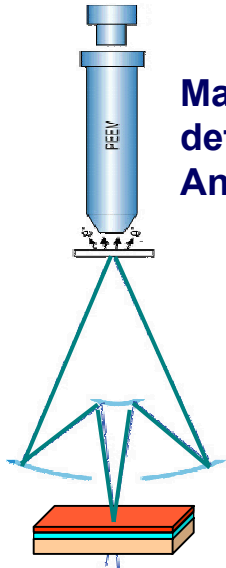
Repair masks using FIB or ebeam

Final inspect & clean

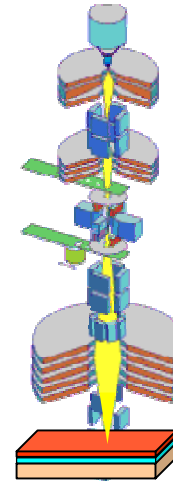
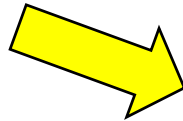
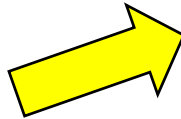
Mount in frame with removable protective cover



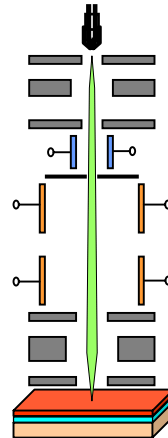
# Patterned mask inspection and repair



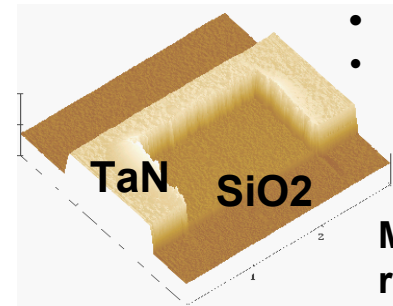
**Mask microscope for  
defect classification  
And inspection**



**Conventional FIB  
metal deposition  
or removal**



**Electron beam  
pattern repair**

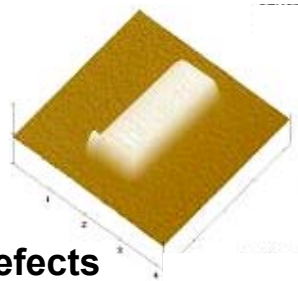


**Electron-Beam Mask Repair**

- Eliminates Ga ion stains
- No ion-beam damage
- High etch selectivity
- Minimizes buffer layers
- ~ 30 nm resolution

**Metal pattern  
removal**

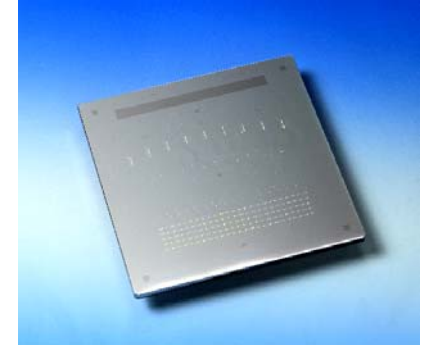
**Metal deposition  
for clear pattern defects**



# Mask Patterning

## Technology;

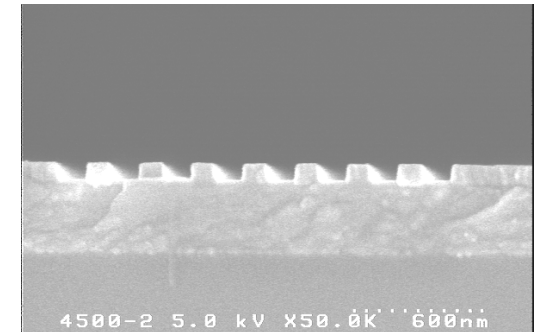
- Variety of absorbers evaluated, Cr and TaN preferred
- Masks patterned using commercial e-beam writing tools
- Two Mask SEMI standards approved, two in process
- Inspection tools demonstrated
- Repair demonstrated using Ga FIB and e-beam etching
- Large k1 minimizes need for OPC, simple flare compensation
- Removable pellicle/cover proposed



**152 mm<sup>2</sup>, 4X Dark Field Reflective Masks**

## Commercial status:

- Masks produced by:
  - Company mask shops:  
Intel, Motorola, AMD, IBM, and Infineon
  - Mask companies: RTC, MCoC, DPI
- Standards developed



**120 nm lines/spaces**

## Production needs:

- Inspection and repair equipment
- Continued development of removable pellicle



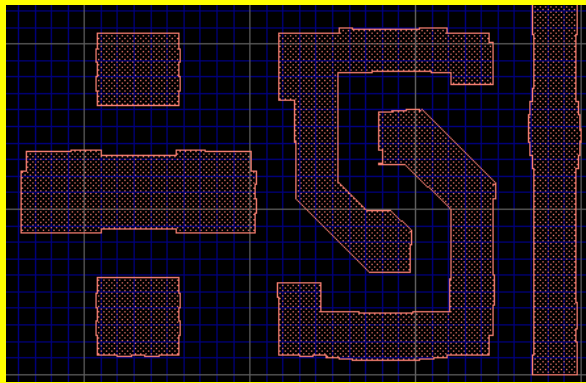
# Estimated EUV & Optical Mask Costs for 45 nm

	<u>Key Attributes</u>	<u>EUV cost relative to optical</u>
Mask blank	flat/defect free	similar Specs. 1.0
Multilayers	multilayer coated	more layers 1.2
Defect inspection	DUV inspection	similar/phase 1.2
Writing time	ebeam, similar CD's	less complex 0.5 – 0.6
Pattern Insp.	DUV inspection	simpler 0.6 – 0.7

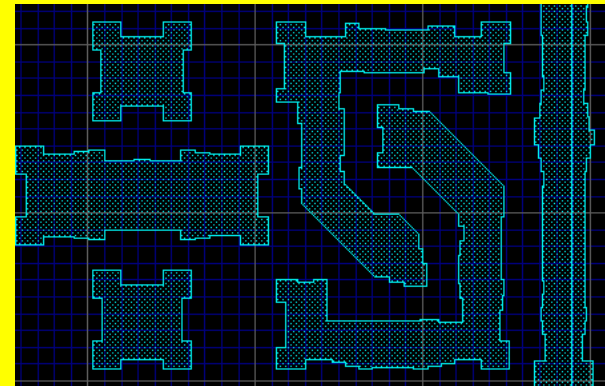
## Estimated costs for 45 nm (equivalent process maturity)

Optical - OPC only	\$ 100 k
OPC & complementary	\$ 150 k
EUV	\$ 43 - \$90 k

**EUV mask**



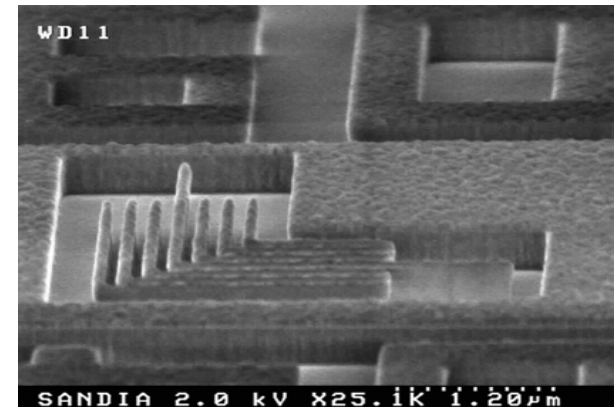
**Optical Mask with OPC**



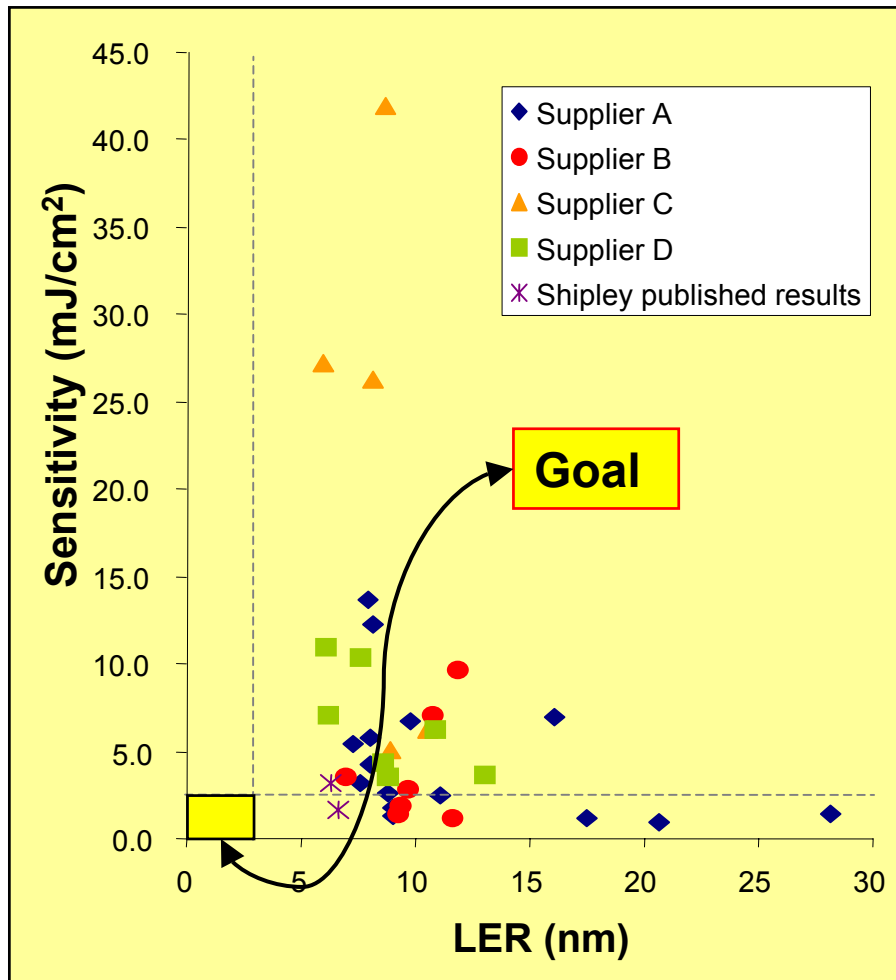
# Resists

## *Approach*

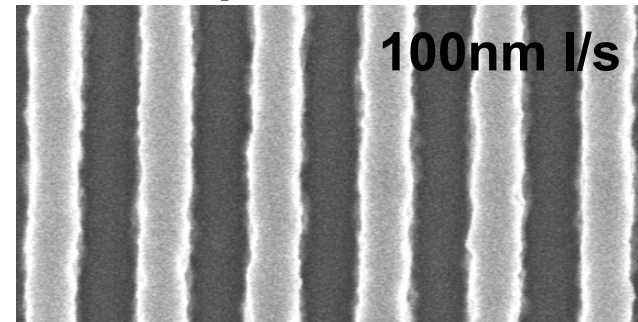
- Extend chemically amplified deep UV resists
- Use Ultra thin resists (UTR)
- Evaluate single layer and bilayer resists



# Resist LER Needs Improvement

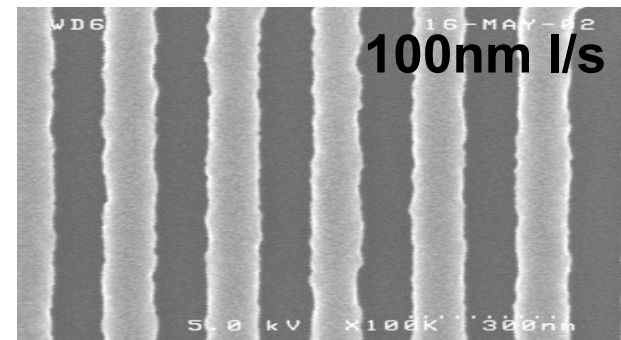


## Best positive resist



Dose=2.3 mJ/cm<sup>2</sup> LER=7.2 nm

## Best negative resist

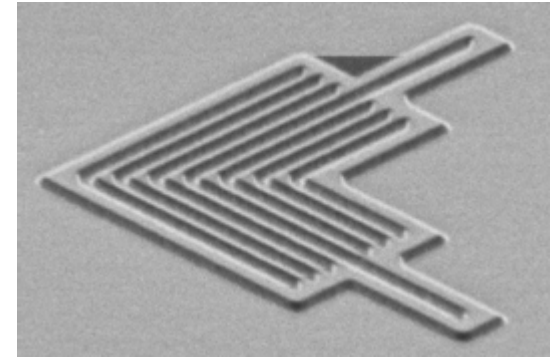


Dose=3.2 mJ/cm<sup>2</sup> LER= 7.6nm

# Resist Development

## Technology;

- Both single layer and bilayer resists demonstrated
- DUV ultra thin resists viable  $> 85$  nm
- Resist sensitivities demonstrated down to  $\sim 2.0$  mJ/cm<sup>2</sup> , LER 5 – 7 nm
- Pattern transfer into hard masks demonstrated
- Flare understood - compensation methods available

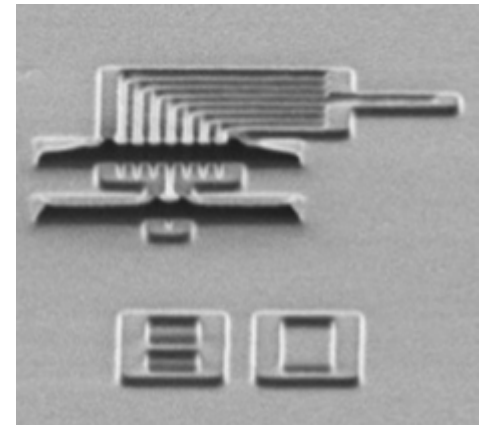


## Commercialization status:

- Companies actively developing resists  
Shipley, JSR, TOK

## Production Needs:

- Reduced LER and improved sensitivity



# World wide EUVL commercialization focus

## Japan

> 10 Companies

Consortia:

- ASET
- EUVA
- MIRAI



## Europe

> 50 Commercial Cos.

Consortia:

- PREUVE
- MEDEA+
- LETI
- IMEC

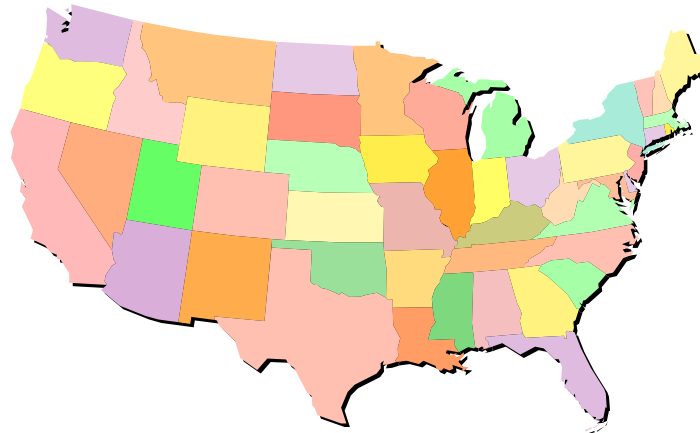


## US

> 40 Commercial companies

Consortia:

- EUV LLC
- I-SEMATECH
- VNL RDC
- SRC



# Remaining challenges

## *Lithography tools with acceptable CoO*

	Present	Required
Beta tool schedule	2006 - 2007	2005 -2006
Source Output (at intermediate focus)	< 10 Watts	>100 Watts
Optics/Illuminator lifetime	TBD	>5 Yrs/>1 Yr
Optics figure and finish	~25 nm rms	<14 nm rms
Multilayer reflectivity (optics)	~65%	>70 %
Production throughput – 300 mm wafers	-----	>80 wph

## *Resists*

LER ( $3\sigma$ )	7 nm @ 2.5 mJ	3 nm @ 2.5 mJ
Resolution/Sensitivity (Printing/dose)	40 nm/5 mJ	<20 nm/2.5 mJ

## *Masks*

Blank flatness	200 nm	50 nm
Blank defect levels (@50 nm)	0.04/cm <sup>2</sup>	0.003/cm <sup>2</sup>
Inspection (blanks and patterned wafers)	70 nm defects	30 nm defects
CD measurements	70 nm	30 nm



# Summary

**EUVL is the only viable solution for 45 nm**

- **Integration of all EUVL modules demonstrated feasibility of the EUVL technology**
- **Mask costs are affordable – defect mitigation and repair methods demonstrated**
- **Suppliers are engaged to commercialize the technology**
- **Remaining technical challenges have been identified and are actively being addressed**
- **Commercialization emphasis is required**